

IN THE CLAIMS:

We claim:

1 1. A memory system comprising a plurality of memory cells arranged in an array
2 and fabricated over a silicon carbide (SiC) substrate.

1 2. The memory system according to Claim 1, wherein the plurality of memory
2 cells are a plurality of T-RAM memory cells.

1 3. The memory system according to Claim 2, wherein each of the plurality of T-
2 RAM memory cells include a first and a second vertical device, where the first vertical
3 device of each of the plurality of T-RAM memory cells is a thyristor and the second vertical
4 device of each of the plurality of T-RAM memory cells is a transfer gate.

1 4. The memory system according to Claim 3, wherein the two vertical devices
2 are connected by an n+ region.

1 5. The memory system according to Claim 2, wherein each of the plurality of T-
2 RAM memory cells has a size of less than or equal to $6F^2$.

1 6. The memory system according to Claim 2, wherein each of the plurality of T-
2 RAM memory cells includes two vertical devices having approximately the same height.

1 7. The memory system according to Claim 1, wherein each of the plurality of
2 memory cells is configured for being operational at high temperatures and in high radiation
3 prone environments.

1 8. The memory system according to Claim 7, wherein each of the plurality of
2 memory cells is operational in a temperature range from 200 to 1000 degrees Celsius.

1 9. The memory system according to Claim 1, wherein each of the plurality of
2 memory cells has a planar cell structure.

1 10. The memory system according to Claim 1, wherein the SiC substrate is a p-
2 type SiC substrate.

1 11. A T-RAM array comprising a plurality of memory cells fabricated over a
2 silicon carbide (SiC) substrate.

1 12. The array according to Claim 11, wherein the SiC substrate is a p-type SiC
2 substrate.

1 13. The array according to Claim 11, wherein the plurality of memory cells are a
2 plurality of T-RAM memory cells.

1 14. The array according to Claim 13, wherein each of the plurality of T-RAM
2 memory cells includes two vertical devices having approximately the same height.

1 15. The array according to Claim 13, wherein a first vertical device of each of the
2 plurality of T-RAM memory cells is a thyristor and a second vertical device of each of the
3 plurality of T-RAM memory cells is a transfer gate.

1 16. The array according to Claim 13, wherein each of the plurality of T-RAM
2 memory cells has a size of less than or equal to $6F^2$.

1 17. The array according to Claim 11, wherein each of the plurality of memory
2 cells is configured for being operational at high temperatures and in high radiation prone
3 environments.

1 18. The array according to Claim 17, wherein each of the plurality of memory
2 cells is operational in a temperature range from 200 to 1000 degrees Celsius.

1 19. The array according to Claim 14, wherein the two vertical devices are
2 connected by an n⁺ region.

1 20. The array according to Claim 11, wherein each of the plurality of memory
2 cells has a planar cell structure.

1 21. A method for fabricating a memory array having a plurality of memory cells,
2 the method comprising the steps of:
3 providing a wafer having at least one silicon carbide (SiC) layer; and
4 fabricating each of the plurality of memory cells over the at least one SiC layer.

1 22. The method according to Claim 21, wherein the plurality of memory cells are
2 a plurality of T-RAM memory cells.

1 23. The method according to Claim 22, wherein each of the plurality of T-RAM
2 cells has a size of less than or equal to $6F^2$.

1 24. The method according to Claim 22, wherein each of the plurality of T-RAM
2 memory cells includes a first portion and a second portion.

1 25. The method according to Claim 24, wherein the first portion is a thyristor and
2 the second portion is a transfer gate.

1 26. The method according to Claim 21, further comprising the step of
2 encapsulating each of the plurality of memory cells with an insulating material.

1 27. The method according to Claim 21, further comprising the step of fabricating
2 each of the plurality of memory cells with a planar cell structure.

1 28. The method according to Claim 21, further comprising the step of providing
2 three layers on the wafer prior to the fabricating step, wherein a first layer is provided on top

1 of the at least one SiC layer and is an n-type layer, a second layer is provided on top of the
2 first layer and is a p-type layer, and a third layer is provided on top of the second layer and is
3 an n-type layer.

1 29. The method according to Claim 21, wherein the step of fabricating each of the
2 plurality of memory cells on the wafer includes the steps of:

3 doping portions of the wafer with a first doping implant; and
4 doping portions of the wafer in proximity to the portions doped with the first doping
5 implant with a second doping implant.

1 30. The method according to Claim 29, wherein the first doping implants is a p-
2 type doping implant and the second doping implant is an n-type doping implant.

1 31. The method according to Claim 29, wherein the step of doping portions of the
2 wafer with a first doping implant includes the step of using a p-type boron implant at an
3 energy in the range of 0.5 to 2 KeV and a dosage of between $2E14/cm^2$ and $8E14/cm^2$ as the
4 first doping implant.

1 32. The method according to Claim 29, wherein the step of doping portions of the
2 wafer with a second doping implant includes the step of using an n-type arsenic implant at an
3 energy in the range of 2 to 15 KeV and a dosage of between $8E14/cm^2$ and $3E15/cm^2$ as the
4 second doping implant.

1 33. The method according to Claim 21, wherein the wafer includes a first layer
2 formed by implanting an n+ type arsenic implant at an energy in the range of 2 to 15 KeV
3 and a dosage of between $8E14/cm^2$ to $3E15/cm^2$; a second layer formed by epitaxial growth
4 using p-type boron at a dosage of between $4E13/cm^2$ to $1E14/cm^2$; and a third layer formed
5 by epitaxial growth using n- type arsenic at a dosage of between $2E13/cm^2$ to $8E13/cm^2$.

1 34. The method according to Claim 29, further comprising the steps of:
2 providing a first mask to conceal the portions of the wafer doped with the first and

1 second doping implants;
2 etching portions of a first layer of the wafer which are not concealed by the first
3 mask;
4 removing the first mask and depositing a dielectric layer over the wafer; and
5 providing a second mask and etching portions of a second layer of the wafer which
6 are not concealed by the second mask.

1 35. The method according to Claim 34, further comprising the steps of:
2 etching portions of a third layer of the wafer in alignment with the etched portions of
3 the second layer;
4 forming a gate dielectric layer on the wafer and depositing a semiconductor material
5 to form a semiconductor layer over the gate dielectric layer;
6 providing a third mask and etching portions of the semiconductor layer and the gate
7 dielectric layer which are not concealed by the third mask; and
8 removing the third mask and etching portions of the second layer of the wafer and the
9 dielectric layer which are not in vertical alignment with the semiconductor layer.

1 36. The method according to Claim 35, further comprising the steps of:
2 oxidizing surfaces which are not in vertical alignment with the semiconductor layer;
3 providing a fourth mask and etching portions of the oxidized surfaces and the third
4 layer of the wafer which are not concealed by the fourth mask to define first and second
5 portions of each of the plurality of memory cells;
6 providing a vertically aligned contact in the first and second portions of each of the
7 plurality of memory cells; and
8 adding an insulating material to encapsulate the first and second portions of each of
9 the plurality of memory cells and to provide a planar structure for the array.

1 37. The method according to Claim 36, further comprising the steps of:
2 forming a plurality of bitlines traversing the plurality of memory cells; and
3 forming a plurality of voltage reference lines traversing the plurality of memory cells.

1 38. The method according to Claim 21, wherein the at least one SiC layer is a p-
2 type layer.

1 39. The method according to Claim 21, wherein each of the plurality of memory
2 cells is configured for being operational at high temperatures and in high radiation prone
3 environments.

1 40. The method according to Claim 39, wherein each of the plurality of memory
2 cells is operational in a temperature range from 200 to 1000 degrees Celsius.